CLAIMS

1. A silicon carbide semiconductor apparatus, comprising:

a first deposition film (2) of low concentration silicon carbide of a first conductivity type formed on a surface of a high concentration silicon carbide substrate (1) of a first conductivity type;

a second deposition film (31) formed on the first deposition film (2) comprising a high concentration gate region of a second conductivity type having a selectively removed first region;

a third deposition film (32) formed on the second deposition film (31) comprising a second region that is wider than the selectively removed first region, a high concentration source region (5) of a first conductivity type and a low concentration gate region of a second conductivity type;

a low concentration base region (4) of a first conductivity type formed in contact with the first deposition film (2) in the first and second regions;

a gate insulation film (6) formed on at least a surface of the third deposition film (32);

a gate electrode (7) formed via the gate insulation film (6);

a drain electrode (10) having a low-resistance contact connection with a backside of the silicon carbide substrate of a first conductivity type; and

a source electrode (9) having a low-resistance contact connection with part of the high concentration source region (5) of a first conductivity type and the low concentration gate region (32) of a second conductivity type.

2. A silicon carbide semiconductor apparatus according to claim 1, wherein the third deposition film (32) has a thickness within a range of 0.2 μm to 0.7 μm and wherein the low concentration gate region (11) of a

second conductivity type selectively formed in the third deposition film (32) has a portion that is in contact with the gate insulation film (6) and has an impurity concentration higher than 1 x 10^{15} cm^{-3} and lower than 5 x 10^{15} cm^{-3}.

3. A silicon carbide semiconductor apparatus according to claim 1 or 2, wherein the low concentration base region (4) of a first conductivity type has an upper surface having at least a portion thereof in contact with the gate insulation film (6) and provided therein with a cavity (41).

4. A silicon carbide semiconductor apparatus according to any of claims 1 to 3, wherein the low concentration base region (4) of a first conductivity type has a lower impurity concentration than the high concentration gate region (31) of a second conductivity type.

5. A silicon carbide semiconductor apparatus according to any of claims 1 to 4, wherein the low concentration gate region (11) of a second conductivity type selectively formed in the third deposition film (32) has a portion that is in contact with the gate insulation film (6) and has an impurity concentration of not higher than 2 x 10^{16} cm^{-3}.

6. A silicon carbide semiconductor apparatus according to any of claims 1 to 5, wherein the low concentration base region (4) of a first conductivity type selectively formed in the third deposition film (32) has a portion that is in contact with the high concentration gate region (31) of a second conductivity type and has an impurity concentration of not higher than 4 x 10^{16} cm^{-3}.

7. A silicon carbide semiconductor apparatus according to any of claims 1 to 6, wherein the high concentration gate region (31) of a second conductivity type is the second deposition film (31) of silicon

carbide formed on the first deposition film (2).

8. A silicon carbide semiconductor apparatus according to any of claims 1 to 7, wherein the gate insulation film (6) formed on the third deposition film has at least a portion thicker than other portions on the low concentration base region (4) of a first conductivity type selectively formed in the third deposition film (32).

9. A silicon carbide semiconductor apparatus according to any of claims 1 to 8, wherein above a surface of the base region (4) of a first conductivity type selectively formed in the third deposition film (32), the gate electrode (7) has at least a portion removed.

10. A silicon carbide semiconductor apparatus according to any of claims 1 to 9, wherein in terms of crystal Miller index the surface of the silicon carbide substrate (1) of a first conductivity type is a plane that is parallel to a (11-20) plane.

11. A silicon carbide semiconductor apparatus according to any of claims 1 to 10, wherein in terms of crystal Miller index the surface of the silicon carbide substrate (1) of a first conductivity type is a plane that is parallel to a (000-1) plane.

12. A silicon carbide semiconductor apparatus according to any of claims 1 to 11, wherein the low concentration gate region (11) of a second conductivity type has a portion that is in contact with the gate insulation film (6) and has a buried channel region (91) of a first conductivity type.

13. A silicon carbide semiconductor apparatus, comprising:

a lower deposition film (2) of low concentration silicon carbide of a

first conductivity type formed on a surface of a high concentration silicon carbide substrate (1) of a first conductivity type;

a high concentration gate region (31) of a second conductivity type selectively formed in the lower deposition film (2) so that a first region of low concentration silicon carbide of a first conductivity type remains in the lower deposition film;

an upper deposition film (32) on the lower deposition film (2), comprising a low concentration base region (4) of a first conductivity type that is a second region wider than the first region, a high concentration source region (5) of a first conductivity type and a low concentration gate region (11) of a second conductivity type;

a gate insulation film (6) formed on at least a surface of the upper deposition film (32);

a gate electrode (7) formed via the gate insulation film (6);

a drain electrode (10) having a low-resistance contact connection with a backside of the silicon carbide substrate (1) of a first conductivity type; and

a source electrode (9) having a low-resistance contact connection with part of the high concentration source region (5) of a first conductivity type and the low concentration gate region (11) of a second conductivity type.

14. A silicon carbide semiconductor apparatus according to claim 13, wherein the upper deposition film (32) has a thickness within a range of 0.2 μm to 0.7 μm and wherein the low concentration gate region (11) of a second conductivity type selectively formed in the upper deposition film (32) has a portion that is in contact with the gate insulation film (6) and has an impurity concentration higher than 1×10^{15} cm^{-3} and lower than 5×10^{15} cm^{-3}.

15. A silicon carbide semiconductor apparatus according to claim 13 or 14, wherein the low concentration base region (4) of a first conductivity type has a lower impurity concentration than the high concentration gate region (51) of a second conductivity type.

16. A silicon carbide semiconductor apparatus according to any of claims 13 to 15, wherein the low concentration gate region (11) of a second conductivity type selectively formed in the upper deposition film (32) has a portion that is in contact with the gate insulation film (6) and has an impurity concentration of not higher than 2×10^{16} cm^{-3}.

17. A silicon carbide semiconductor apparatus according to any of claims 13 to 16, wherein the upper deposition film (32) is constituted of silicon carbide.

18. A silicon carbide semiconductor apparatus according to any of claims 13 to 17, wherein the gate insulation film (6) formed on the upper deposition film (32) has at least a portion that is thicker than other portions on the low concentration base region (4) of a first conductivity type selectively formed in the upper deposition film (32).

19. A silicon carbide semiconductor apparatus according to any of claims 13 to 18, wherein on the surface of the base region (4) of a first conductivity type selectively formed in the upper deposition film (32), the gate electrode (7) has at least a portion removed.

20. A silicon carbide semiconductor apparatus according to any of claims 13 to 19, wherein in terms of crystal Miller index the surface of the silicon carbide substrate (1) of a first conductivity type is a plane that is parallel to a (11-20) plane.

21. A silicon carbide semiconductor apparatus according to any of claims 13 to 20, wherein in terms of crystal Miller index the surface of the silicon carbide substrate (1) of a first conductivity type is a plane that is parallel to a (000-1) plane.

22. A silicon carbide semiconductor apparatus according to any of claims 13 to 21, wherein the low concentration gate region (11) of a second conductivity type has a portion that is in contact with the gate insulation film (6) and has a buried channel region (91) of a first conductivity type.

23. A method of manufacturing a silicon carbide semiconductor apparatus, comprising at least the steps of:

forming a first deposition film (2) of low concentration silicon carbide of a first conductivity type on a surface of a high concentration silicon carbide substrate (1) of a first conductivity type;

forming on the first deposition film (2) a second deposition film (31) having a first region from which a high concentration region of a second conductivity type has been selectively removed;

forming on the second deposition film (31) and on the selectively removed first region a third deposition film (32) comprised of a low concentration region of a second conductivity type;

selectively forming a second region in the third deposition film (32) that is wider than the first region by forming a low concentration base region (4) of a first conductivity type in the first and second regions in contact with the first deposition film (2) of low concentration silicon carbide of a first conductivity type, and selectively forming a source region (5) constituted of a high concentration of silicon carbide of a first conductivity type in the third deposition film (32);

forming a gate insulation film (6) on at least the surface of the third deposition film (32);

forming a gate electrode (7) via the gate insulation film (6);

forming a drain electrode (10) having a low-resistance contact connection on a backside of the silicon carbide substrate (1) of a first conductivity type; and

forming a source electrode (8) having a low-resistance contact connection with part of the high concentration source region (9) of a first conductivity type and the low concentration gate region (11) of a second conductivity type.

24. A method of manufacturing a silicon carbide semiconductor apparatus according to claim 23, comprising the steps of:

forming the second deposition film (31) on the first deposition film (2);

forming a trench (41) that extends from the surface of the second deposition film (31) to the first deposition film (2);

forming the third deposition film (32) on the second deposition film (31) and the trench (41); and

selectively implanting impurity ions of a first conductivity type to form the low concentration base region (4) of a first conductivity type in the third deposition film (32).

25. A method of manufacturing a silicon carbide semiconductor apparatus, comprising at least the steps of:

forming a lower deposition film (2) of low concentration silicon carbide of a first conductivity type on a surface of a silicon carbide substrate (1) of a first conductivity type;

forming an impurity region (31) of a second conductivity type in the lower deposition film (2);

forming an upper deposition film (32) constituting a low concentration gate region (11) of a second conductivity type on the lower deposition film (2) in which the impurity region (31) of a second

conductivity type is formed;

forming a high concentration source region (5) of a first conductivity type on the upper deposition film (32);

forming in the upper deposition film (32) a low concentration base region (4) of a first conductivity type in contact with the lower deposition film (2);

forming a gate insulation film (6) on at least a surface of the upper deposition film (32);

forming a gate electrode (7) via the gate insulation film (6);

forming a drain electrode (10) having a low-resistance contact connection with a backside of the silicon carbide substrate (1) of a first conductivity type; and

forming a source electrode (9) having a low-resistance contact connection with part of the high concentration source region (5) of a first conductivity type and the low concentration gate region (11) of a second conductivity type.

26. A method of manufacturing a silicon carbide semiconductor apparatus according to claim 25, comprising the steps of:

forming the impurity region of a second conductivity type in the lower deposition film (2) of low concentration silicon carbide by implantation of a high concentration of impurity ions of a second conductivity type, and forming the upper deposition film (32) thereon; and

selectively implanting impurity ions of a first conductivity type in the upper deposition film (32) to form the low concentration base region (4) of a first conductivity type.